AMENDMENTS TO THE SPECIFICATION

Page 4, sixth full paragraph, please replace it with the following amended paragraph:

figures ~~1A-1F~~ 1A-1G are schematic diagrams of one embodiment of the invention that allows definition of source and drain electrode of a planar FET with high resolution.

Page 7, second full paragraph, please replace it with the following amended paragraph:

After forming the source and drain electrodes 9, 10 in this way the device is completed by depositing a layer of semiconducting material 11, such as regioregular poly(3-hexylthiopene) (P3HT) or poly(dioctylfluorene-co-bithiophene) (F8T2), a layer of gate dielectric 12, such as a polymer layer of poly(methyimethacrylate (PMMA) and by printing a pattern of conducting material for the gate electrode. The gate electrode 13 can be formed from a conducting polymer such as PEDOT/PSS or a inorganic metal. Both the active semiconductor and the dielectric layer may also be patterned, such as to form an active layer island of the device in order to reduce crosstalk between neighbouring devices, as shown in Fig. 1G.